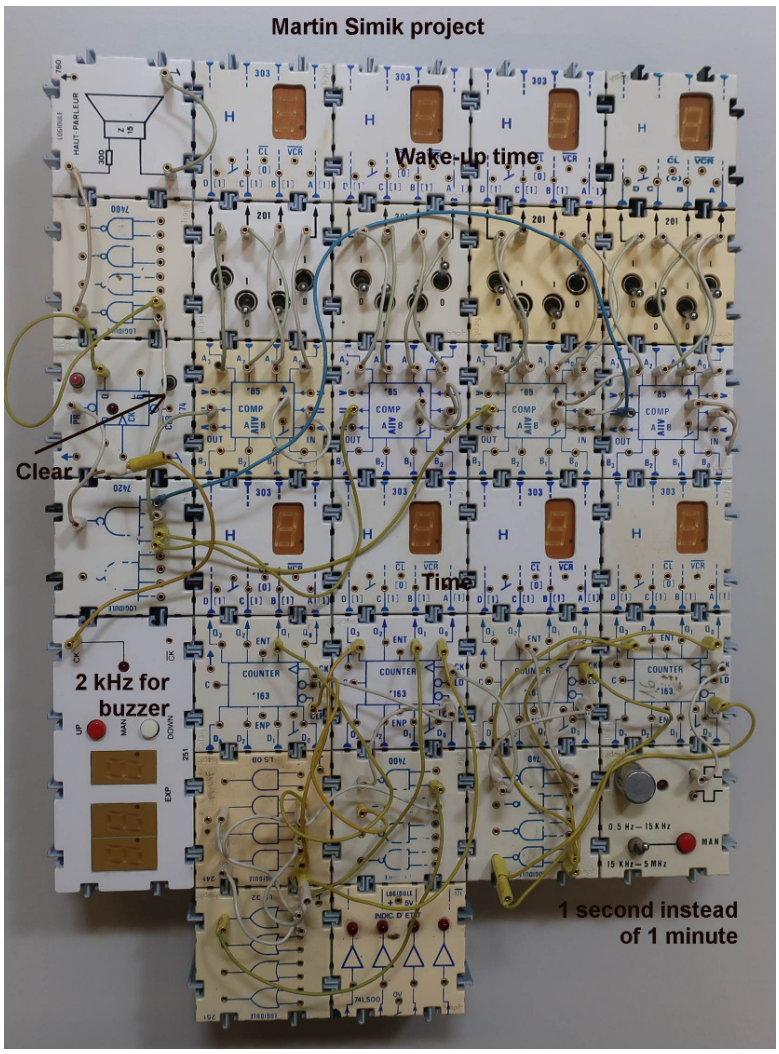
https//www.didel.com/AlarmClock.pdf



Designed and built by Martin Simik, sept 2019, 50e EPFL

How to build an Alarm clock with time set

Clock

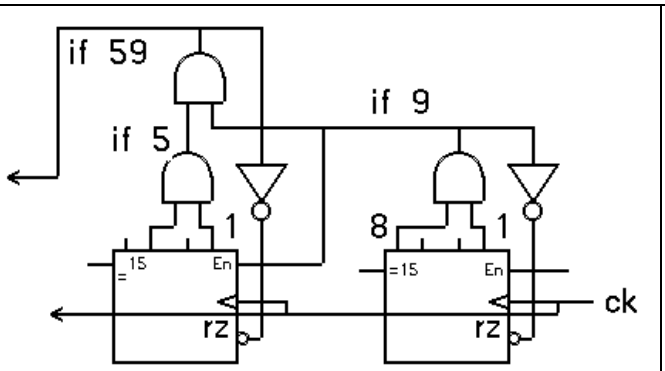
The oscillator has a 1Hz mode (the one on the picture is analogue and cover a wide range of frequencies to quickly set a time).

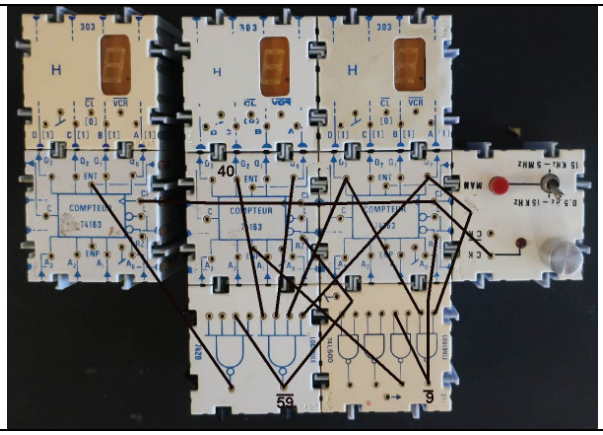
Time Set

The counters have a synchronous parallel mode. All counters need to use the same clock for this purpose. A switch forces /Ld to "0" while time is preset.

Second counter

The schematic is documented on "ModulesLogiques.pdf". Clock in is from the 1Hz oscillator, continuously running. "59" output is the enable for the next counter.
There are always options for implementing the final wiring. Below, AND gates are used on the drawing, but a 4-input NAND gate decode the "59" condition on the test logidules.





Minute and hours counters

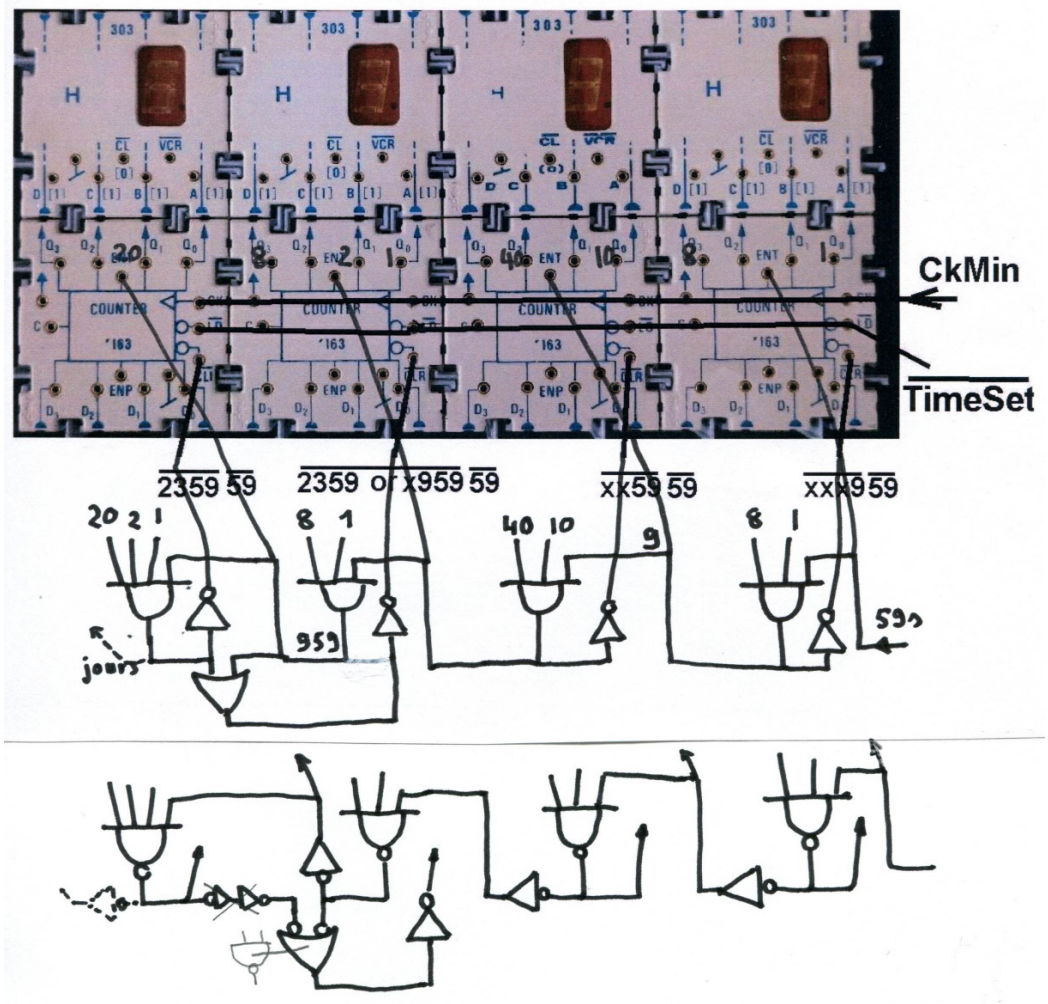
Understanding all the constraints is not so trivial. For all counters we have to provide at clock time a /Clr and /Ld signal.. From the specs, if /Clr and /Ld are both active, /Clr is executed. We cannot simplify the wiring by using independent semi-synchronous modules that divide by 60, 60, 24. It would require switches to send a common clock for set-up.

Logic design

For each counter, we have to think when to clear it and when to increment the next counter. It is indeed the same signal, except the Clr is inverted.

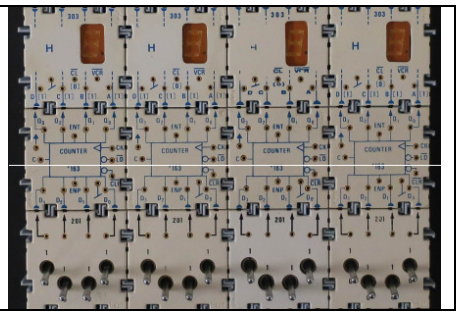
The next picture show all the design steps:

1) Writing some formula for making clear when the reset occurs
2) Drawing the logic diagram with AND/OR/INV
3) Converting for the implementation with logic circuits (deMorgan). Here we decide to use only Nand gates with the advantages that AND and INV are in the same package and makes the wiring more easy.
4) Distribute the gates on well positioned logidules, to maximize short wires and take advantage of the color of longer wires.



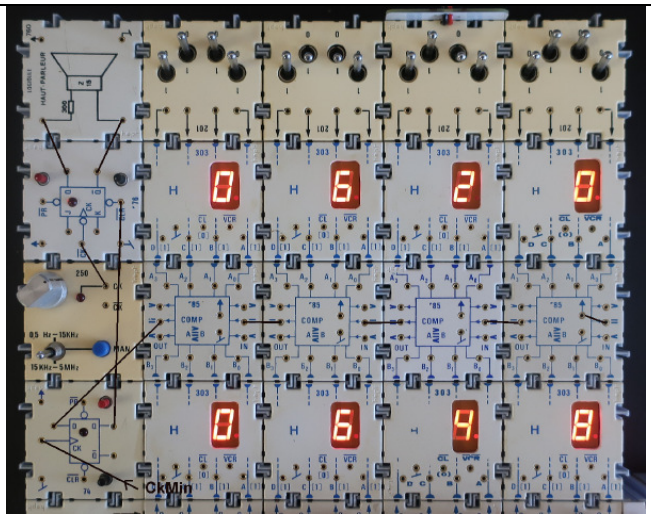
Time set

74LS163 counters have parallel inputs. If /Ld is active, data from switches is loaded and shown on the outputs. But /Clr has priority. This means that if some counter in a state ready to be cleared at next clock, it will be cleared first and then loaded. This is of course only visible during testing with clock send by the push button. With the common clock at 1 Hz, it may take 3 seconds untill time is correctly set.



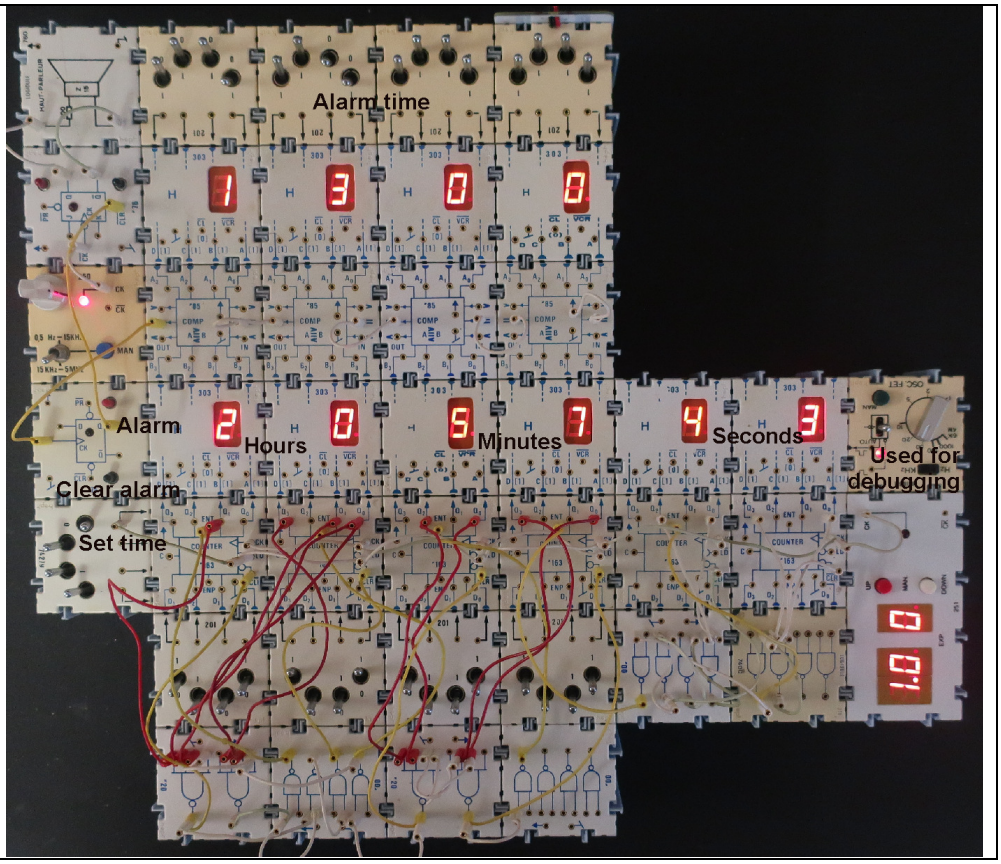
Alarm

Understanding and wiring the comparator is straightforward since we are only interested in equality. Equal value must not trigger a flop-flop, our design is not fully synchronous and there may be glitches. A D-FF triggered by CkMin is required. This FF open a gate that sends some unpleasant sound on the speaker. Notice the oscillator frequency is divided by 2 by the JK flip-flop that play the role of the And gate and amplifier.



Final assembly and part count

6	74LS163 counter
4	74LS85 comparator
8+1	4 bit switches
10	Hex displays
2	74LS20 (2xNand4)
4	74LS00 (4xNand2)
1	1Hz LSL clock
1	Adj clock set at 2Khz
1	D-FF
1	JK-FF
1	Speaker



Jdn 190926